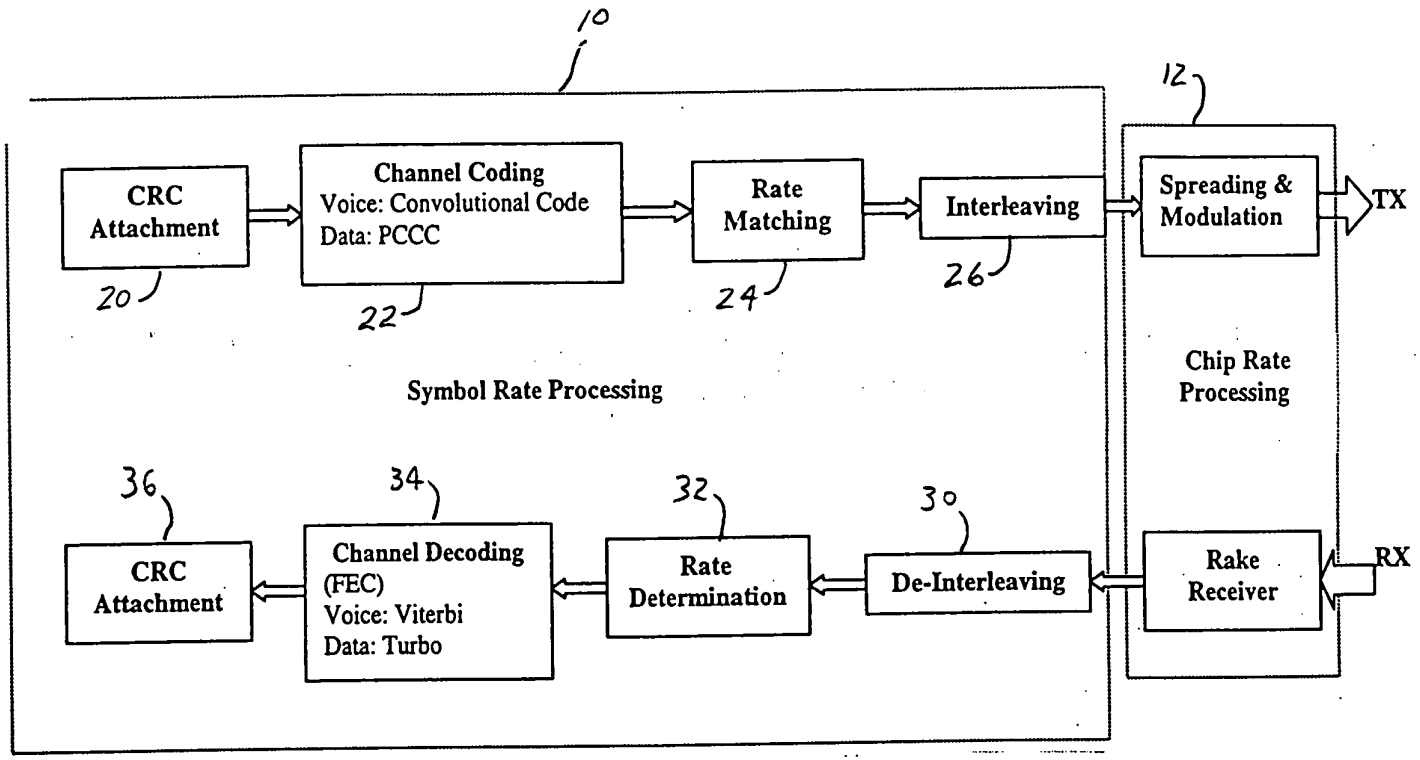

10
12
CRC Attachment
20
Channel Coding
Voice: Convolutional Code
Data: PCCC
22
Rate Matching
24
Interleaving
26
Spreading & Modulation
TX
Symbol Rate Processing
Chip Rate Processing
36
CRC Attachment
34
Channel Decoding
(FEC)
Voice: Viterbi
Data: Turbo
32
Rate Determination
30
De-Interleaving
Rake Receiver
RX

FIG. 1

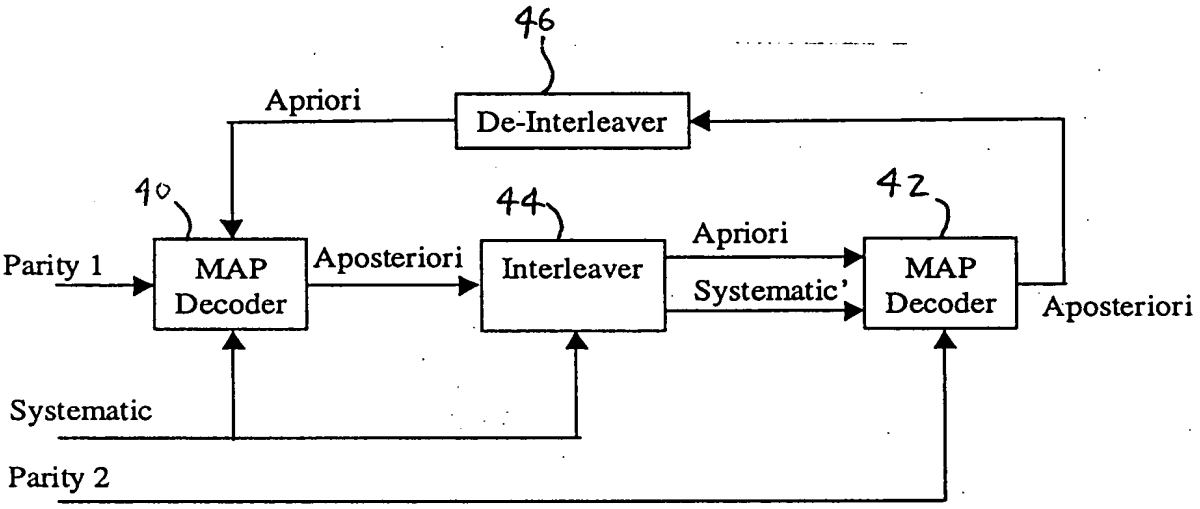

46
Apriori
De-Interleaver
40
44
42
Parity 1
MAP Decoder
Aposteriori
Interleaver
Apriori
Systematic'
MAP Decoder
Aposteriori
Systematic
Parity 2

FIG. 2

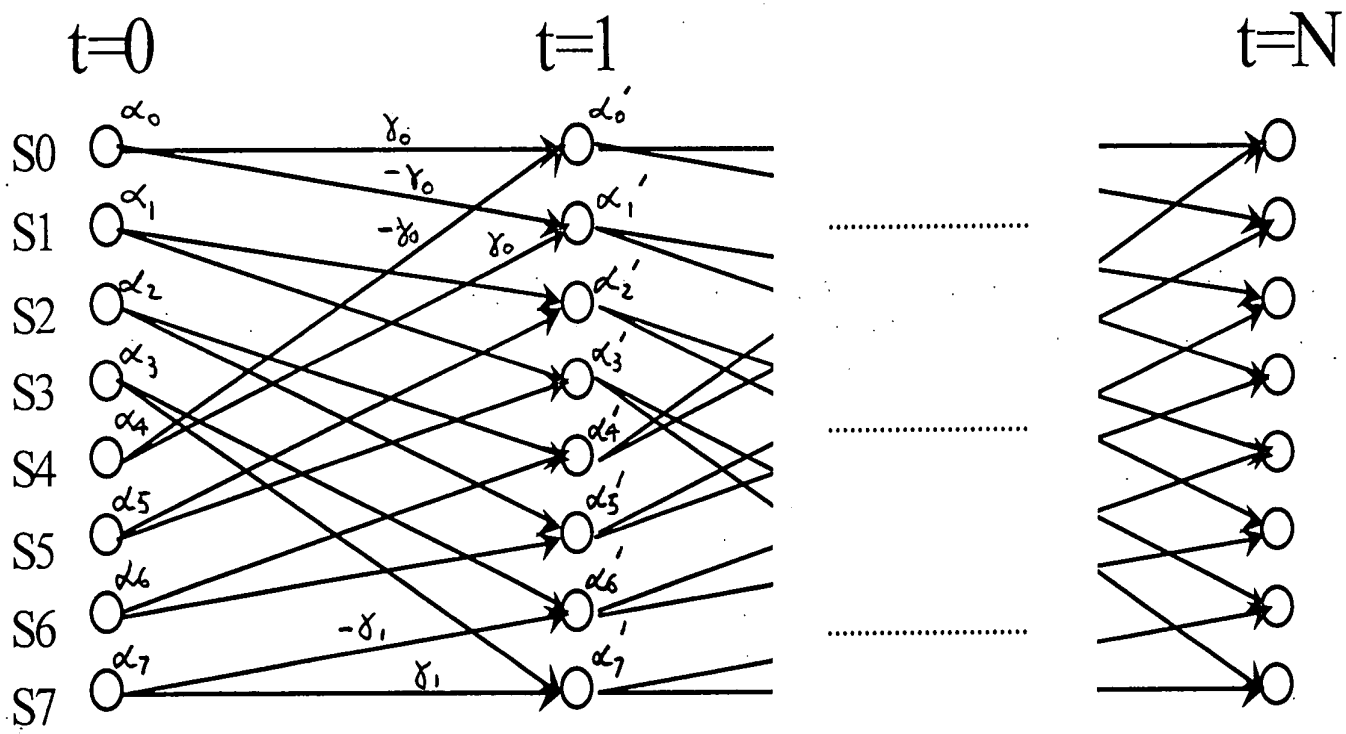


FIG. 3

$$\ln[\alpha_k(s)] = \mathrm{MAX}\{\ln[\alpha_{k-1}(s')]+\ln[\gamma_k(s',s)],\ \ln[\alpha_{k-1}(s'')]-\ln[\gamma_k(s',s)]\} + \ln[1+e^{-\mathrm{abs}(\ln[\alpha_{k-1}(s')]-\ln[\alpha_{k-1}(s'')])}]$$

FIG. 4

$$Ln\left[\beta_{k-1}(s)\right] = MAX\left\{Ln[\beta_k(s')] + Ln[\gamma_k(s',s)]\ ,\ Ln[\beta_k(s'')] - Ln[\gamma_k(s',s)]\right\} + Ln\left[1 + e^{-abs(Ln[\beta_k(s')] - Ln[\beta_k(s'')])}\right]$$

FIG. 5

$$LLR(k) = \underset{S^+}{Max}\{\ln[\alpha(s_{k-1})] + \ln[\gamma(s',s)] + \ln[\beta(s_k)]\}$$

$$- \underset{S^-}{Max}\{\ln[\alpha(s_{k-1})] + \ln[\gamma(s',s)] + \ln[\beta(s_k)]\}$$

$$+ \text{Jacobian Correction Factor}$$

FIG. 6

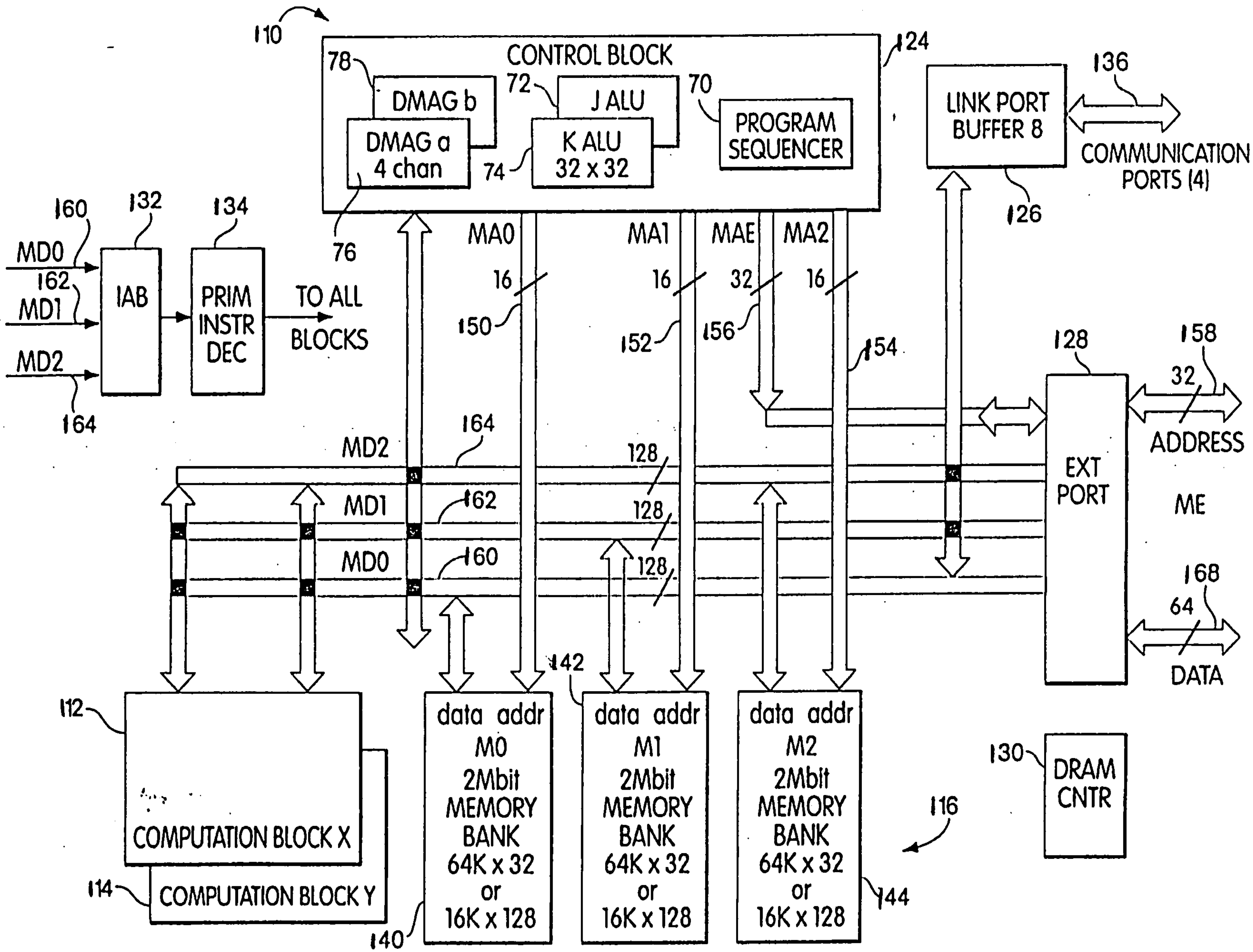

110
CONTROL BLOCK
124
78
DMAG b
DMAG a
4 chan
76
72
J ALU
K ALU
32 x 32
74
70
PROGRAM
SEQUENCER
LINK PORT
BUFFER 8
126
136
COMMUNICATION
PORTS (4)
160
MD0
162
MD1
MD2
164
132
IAB
134
PRIM
INSTR
DEC
TO ALL
BLOCKS
MA0
16
150
MA1
16
152
MAE
32
156
MA2
16
154
128
EXT
PORT
158
32
ADDRESS
ME
168
64
DATA
MD2
164
MD1
162
MD0
160
128
128
128
112
COMPUTATION BLOCK X
114
COMPUTATION BLOCK Y
140
data addr
M0
2Mbit
MEMORY
BANK
64K x 32
or
16K x 128
142
data addr
M1
2Mbit
MEMORY
BANK
64K x 32
or
16K x 128
data addr
M2
2Mbit
MEMORY
BANK
64K x 32
or
16K x 128
144
116
130
DRAM
CNTR

FIG. 7

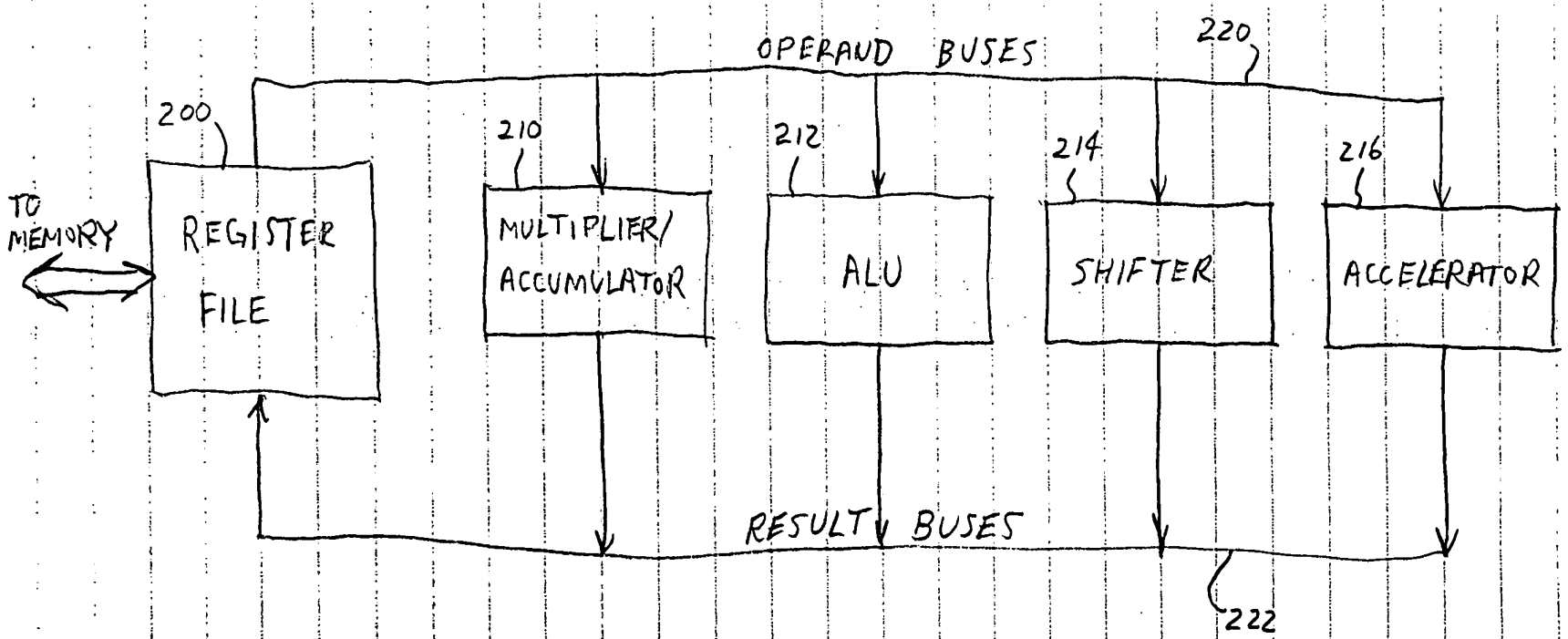
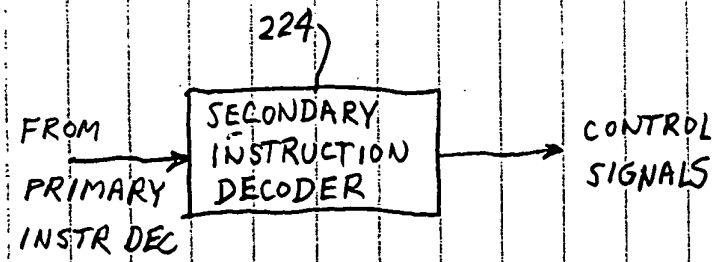


FIG. 8



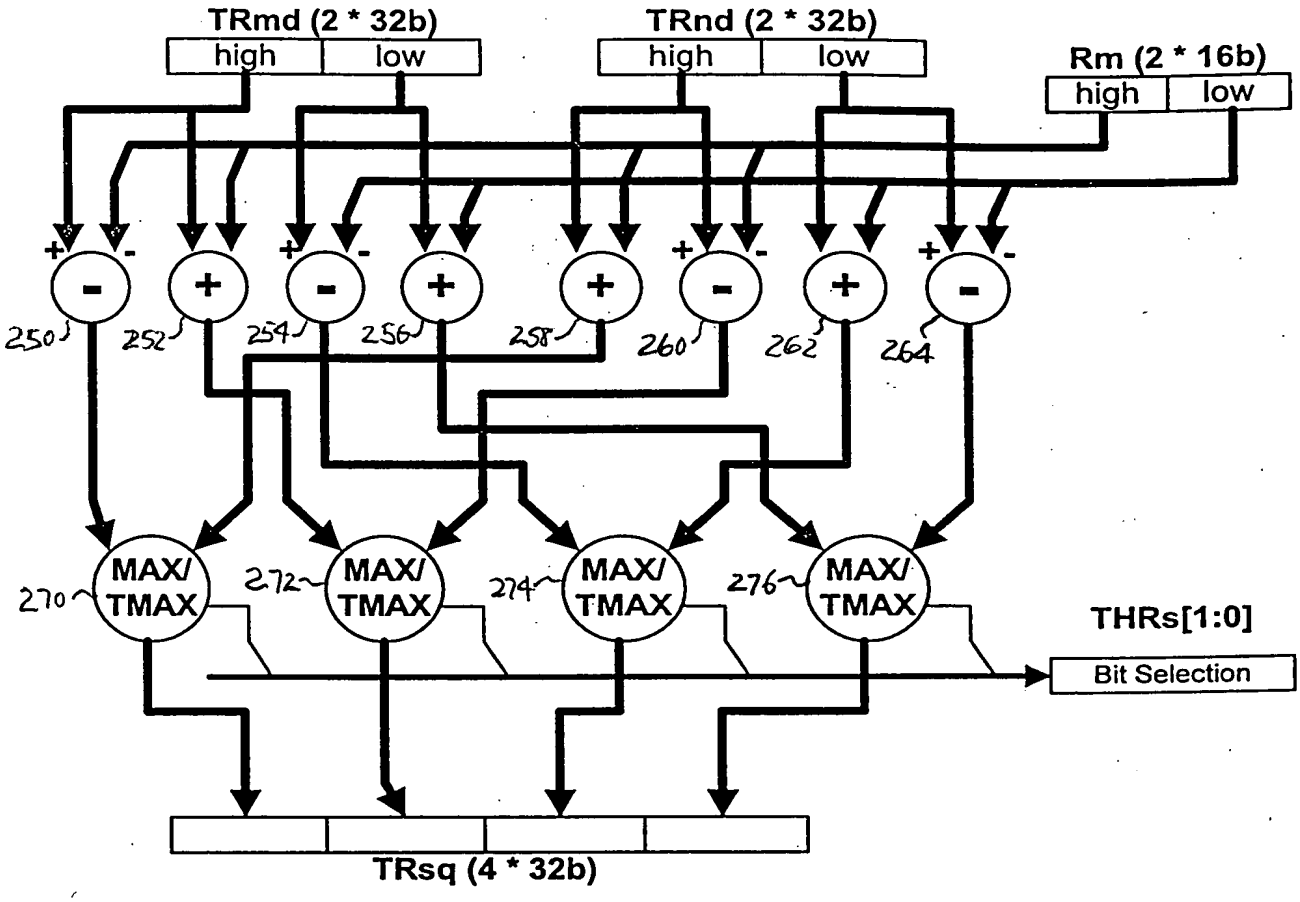

TRmd (2 * 32b)
high
low
TRnd (2 * 32b)
high
low
Rm (2 * 16b)
high
low
250
252
254
256
258
260
262
264
MAX/
TMAX
270
272
274
276
THRs[1:0]
Bit Selection
TRsq (4 * 32b)

FIG. 9

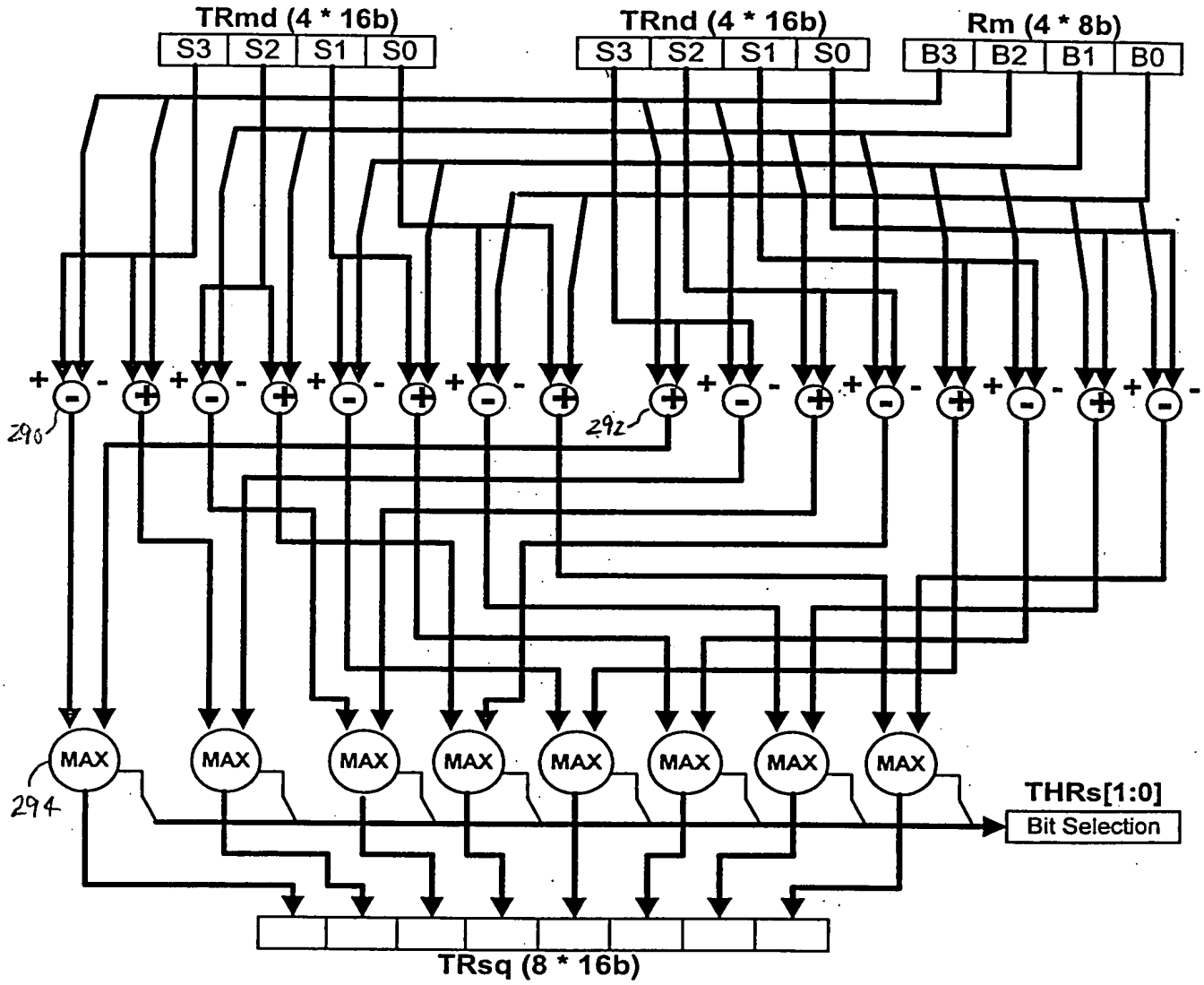

TRmd (4 * 16b)
S3
S2
S1
S0
TRnd (4 * 16b)
S3
S2
S1
S0
Rm (4 * 8b)
B3
B2
B1
B0
290
292
MAX
MAX
MAX
MAX
MAX
MAX
MAX
MAX
294
THRs[1:0]
Bit Selection
TRsq (8 * 16b)

FIG. 10

```
Loop:
R7:4   =TR7:4,   TR11:8  = ACS(TR5:4, TR1:0, sR24);   q[K22+=4]=xR3:0;    q[J22-=4]=yR3:0;;
R11:8  =TR11:8,  TR15:12 = ACS(TR7:6, TR3:2, sR25);   q[K22+=4]=xR7:4;    q[J22-=4]=yR7:4;;

R15:12 =TR15:12,TR3:0    = ACS(TR13:12,TR9:8, sR26); q[K22+=4]=xR11:8;   q[J22-=4]=yR11:8;;
R3:0   =TR3:0,   TR7:4    = ACS(TR15:14,TR11:10,sR27);q[K22+=4]=xR15:12;q[J22-=4]=yR15:12;;

R7:4   =TR7:4,   TR11:8  = ACS(TR5:4, TR1:0, sR28);   q[K22+=4]=xR3:0;    q[J22-=4]=yR3:0;;
R11:8  =TR11:8,  TR15:12 = ACS(TR7:6, TR3:2, sR29);   q[K22+=4]=xR7:4;    q[J22-=4]=yR7:4;;

R15:12 =TR15:12,TR3:0    = ACS(TR13:12,TR9:8, sR30); q[K22+=4]=xR11:8;   q[J22-=4]=yR11:8;;
R3:0   =TR3:0,   TR7:4    = ACS(TR15:14,TR11:10,sR31);q[K22+=4]=xR15:12; q[J22-=4]=yR15:12;;
IF nLOOP jump loop;;
```

FIG. 11

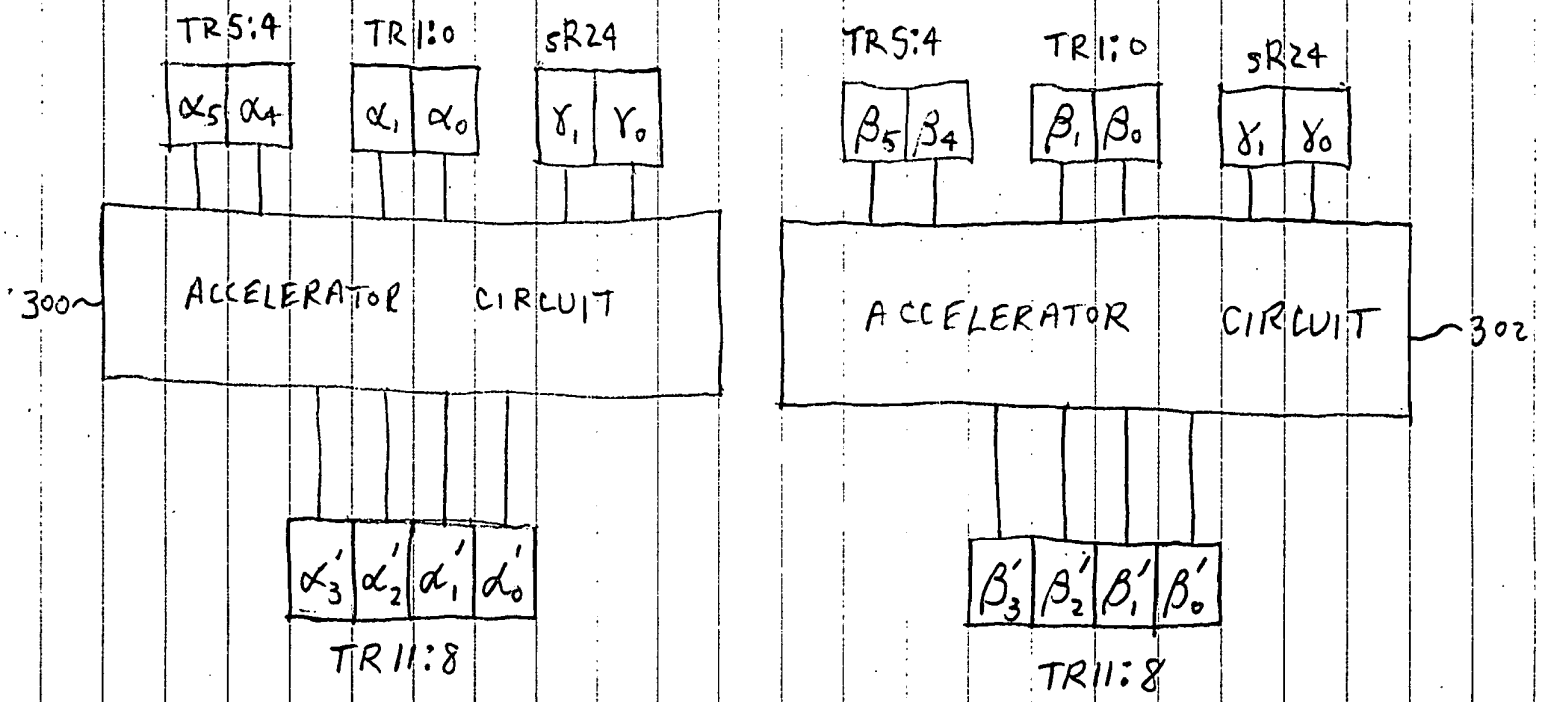


FIG. 12

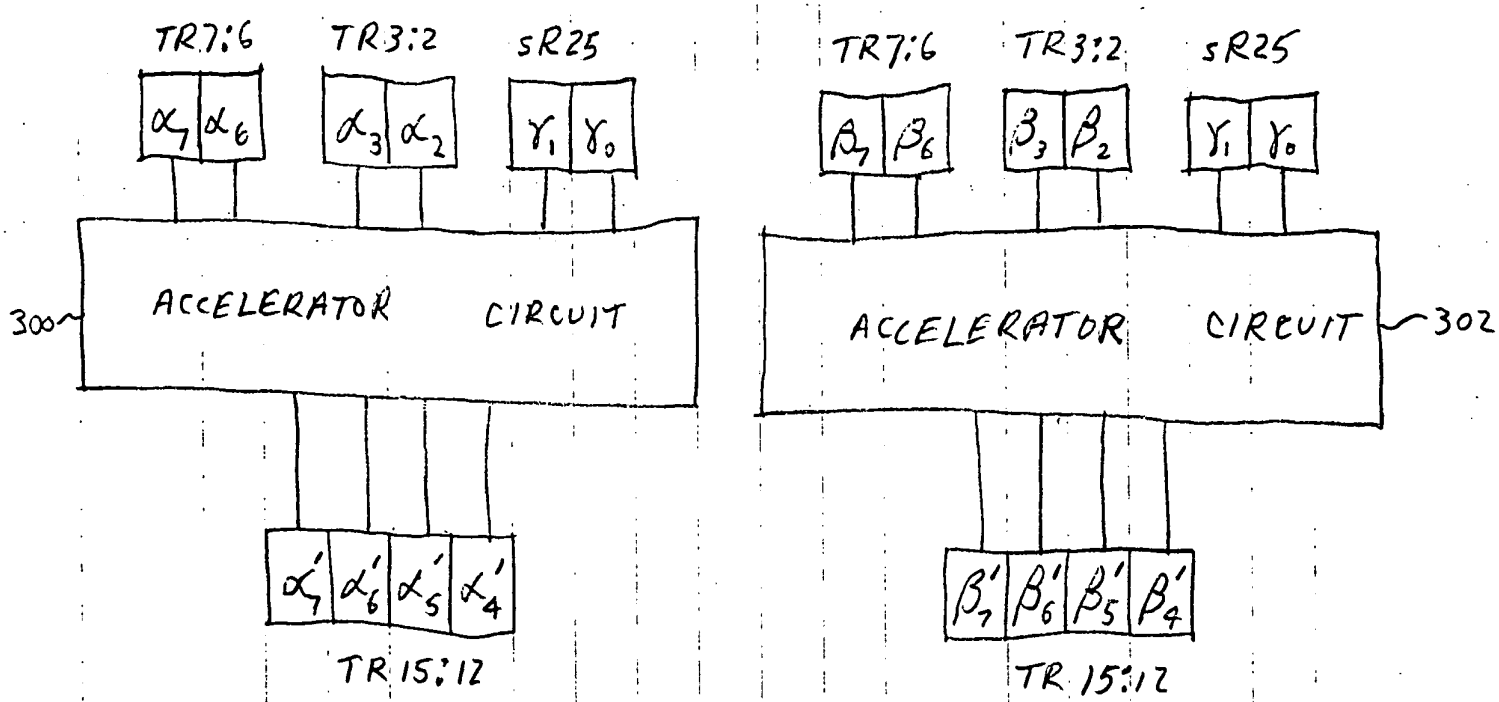

TR7:6
TR3:2
sR25
α_7 α_6
α_3 α_2
γ_1 γ_0
300
ACCELERATOR CIRCUIT
α'_7 α'_6 α'_5 α'_4
TR 15:12
TR7:6
TR3:2
sR25
β_7 β_6
β_3 β_2
γ_1 γ_0
ACCELERATOR CIRCUIT
302
β'_7 β'_6 β'_5 β'_4
TR 15:12

FIG. 13

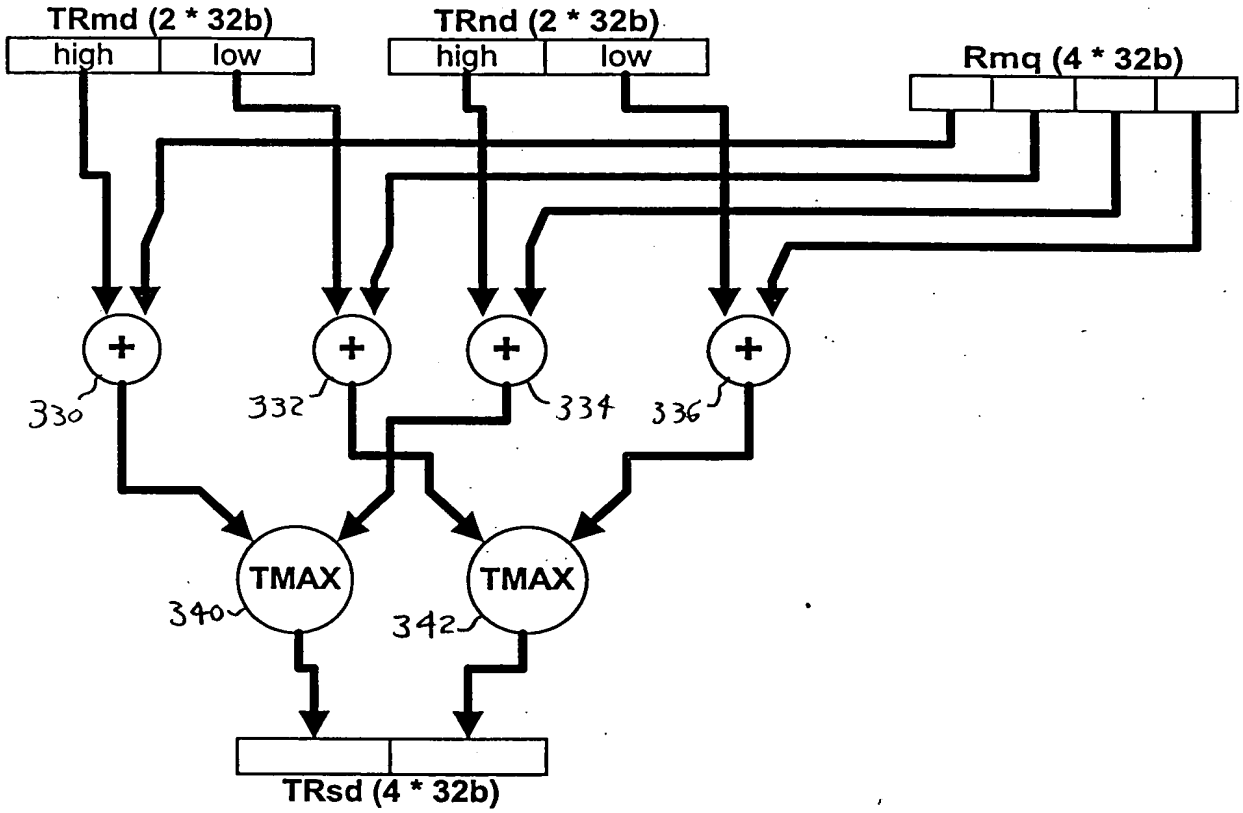

TRmd (2 * 32b)
high
low
TRnd (2 * 32b)
high
low
Rmq (4 * 32b)
+
+
+
+
330
332
334
336
TMAX
TMAX
340
342
TRsd (4 * 32b)

FIG. 14

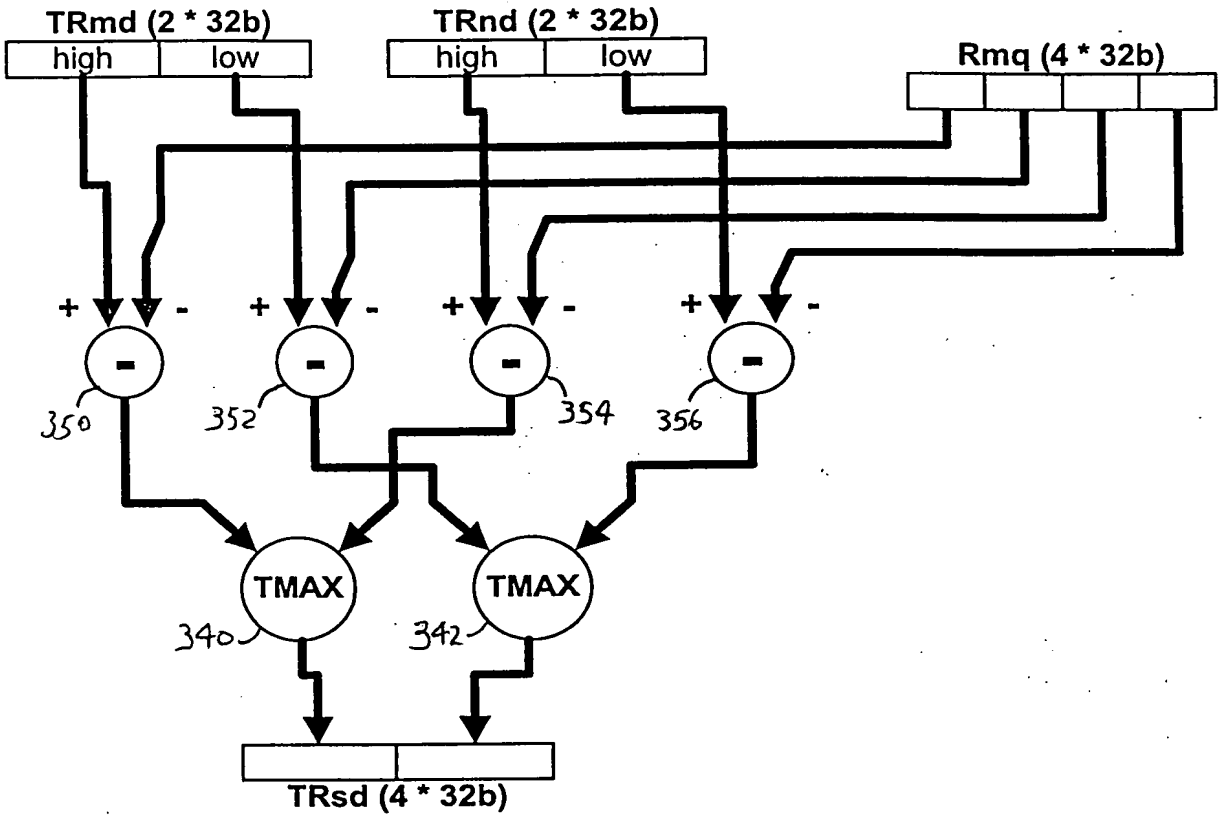

TRmd (2 * 32b)
high
low
TRnd (2 * 32b)
high
low
Rmq (4 * 32b)
+
-
+
-
+
-
+
-
350
352
354
356
TMAX
TMAX
340
342
TRsd (4 * 32b)

FIG. 15

```
//ADD  Alpha + Beta's for 0 and 1 state changes
TR9:8    = TMAX(TR1:0 + R9:8,  TR3:2 + R11:10);;
TR11:0   = TMAX(TR1:0 + R13:12,TR3:2 + R15:14);;
TR13:12  = TMAX(TR5:4 + R13:12,TR7:6 + R15:14);;
TR15:14  = TMAX(TR5:4 + R9:8,  TR7:6 + R11:10);;

//ADD  Gamma for 0 and 1 state changes
TR5:4    = TMAX(TR9:8   + R0:0, TR13:12 + R1:1);;
TR12:11  = TMAX(TR11:10 - R0:0, TR15:14 - R1:1);;

R0       = TMAX(TR5, TR4);;
R1       = TMAX(TR12,TR11);;

R0       = R1 - R0;;
```

FIG.16

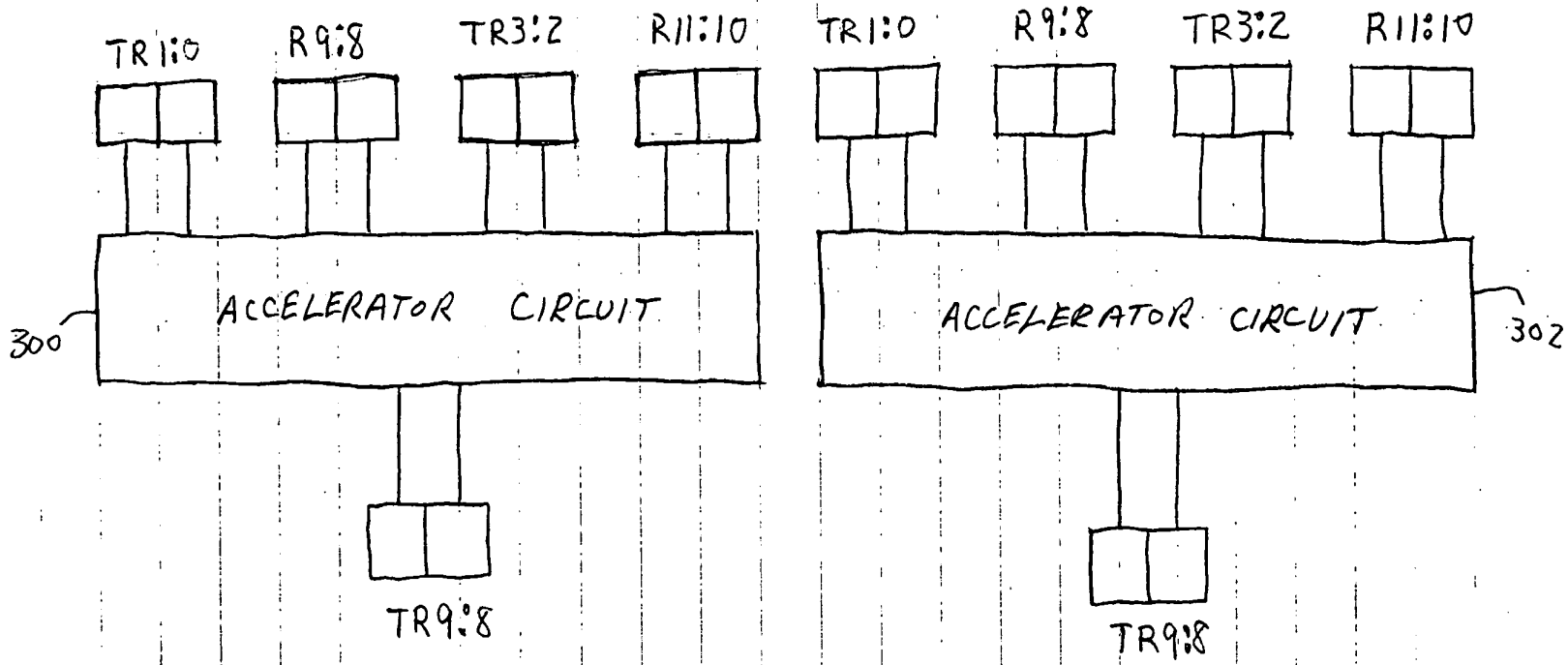

TR1:0
R9:8
TR3:2
R11:10
TR1:0
R9:8
TR3:2
R11:10
ACCELERATOR CIRCUIT
300
ACCELERATOR CIRCUIT
302
TR9:8
TR9:8

FIG.17

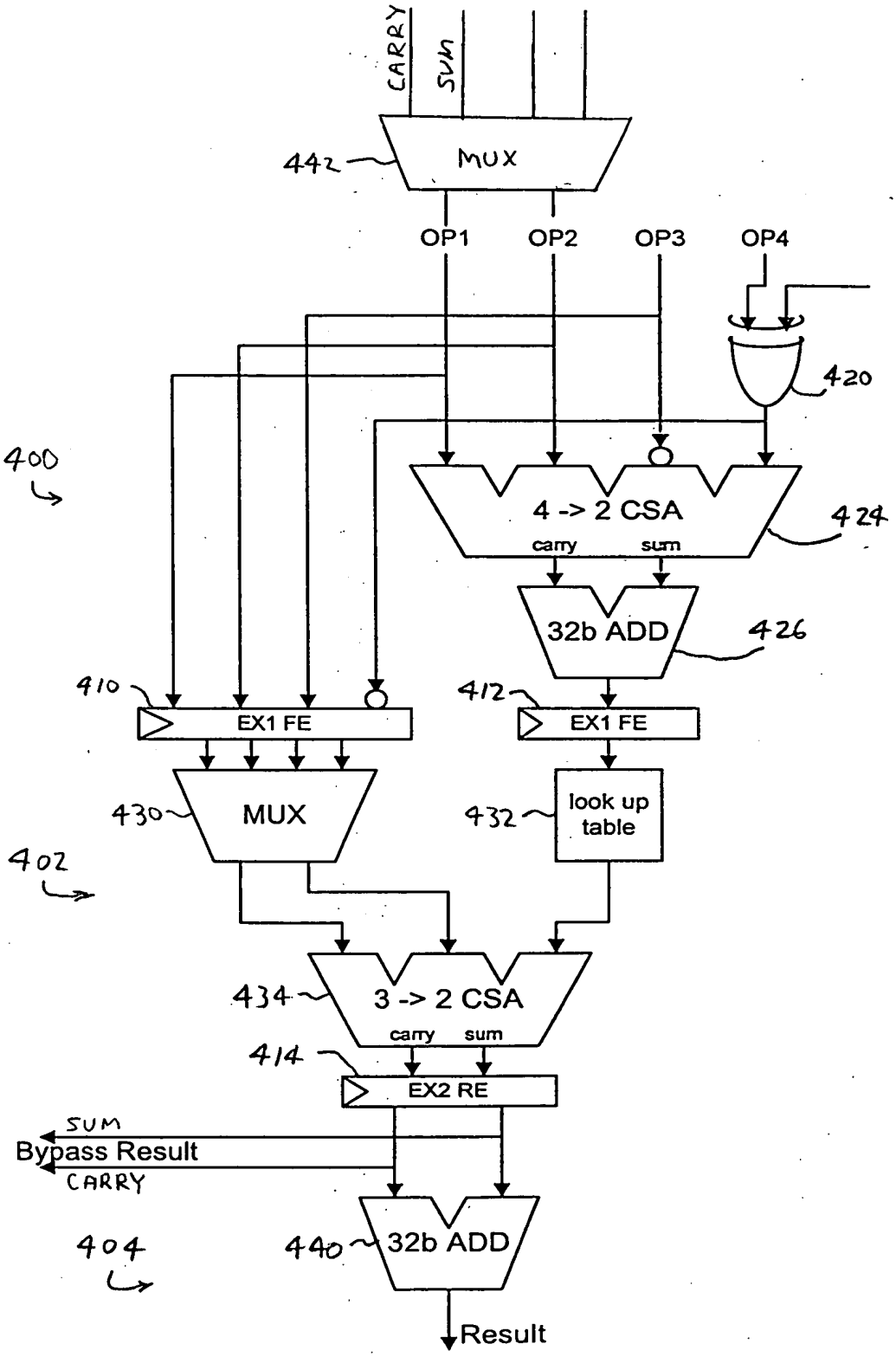

CARRY
SUM
442
MUX
OP1
OP2
OP3
OP4
420
400
4 -> 2 CSA
carry
sum
424
32b ADD
426
410
412
EX1 FE
EX1 FE
430
MUX
432
look up table
402
434
3 -> 2 CSA
carry
sum
414
EX2 RE
SUM
Bypass Result
CARRY
404
440
32b ADD
Result

FIG. 18